

# CEC 450

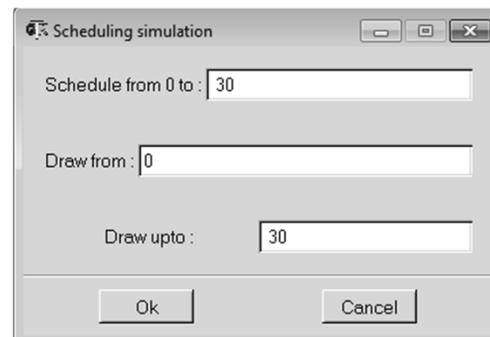
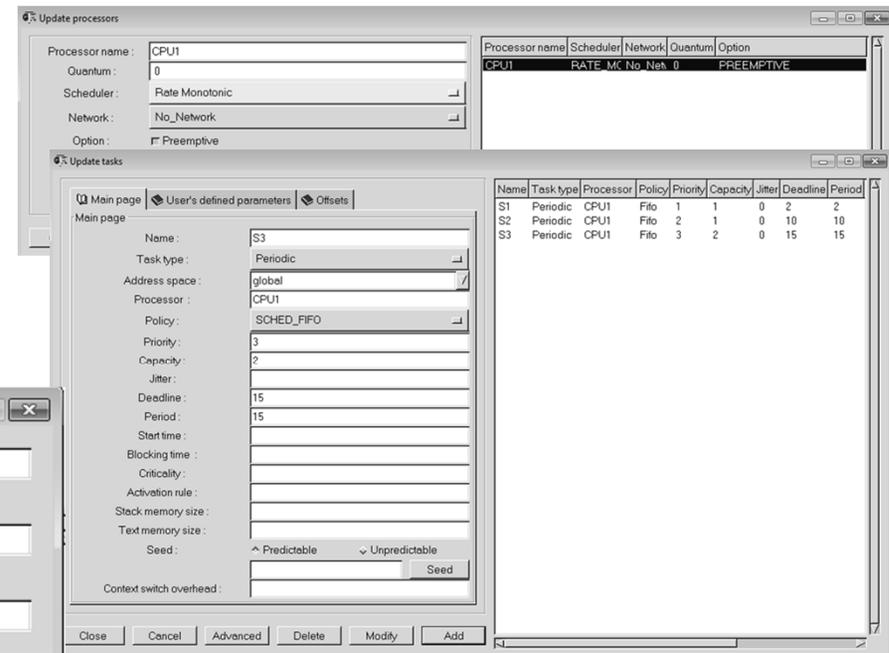
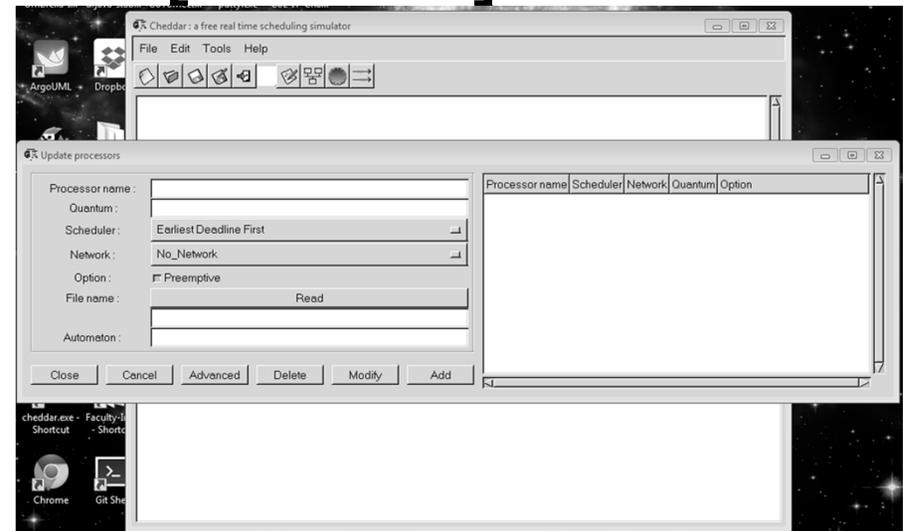
## Real-Time Systems

*Lecture – RM Analysis Examples with Cheddar*



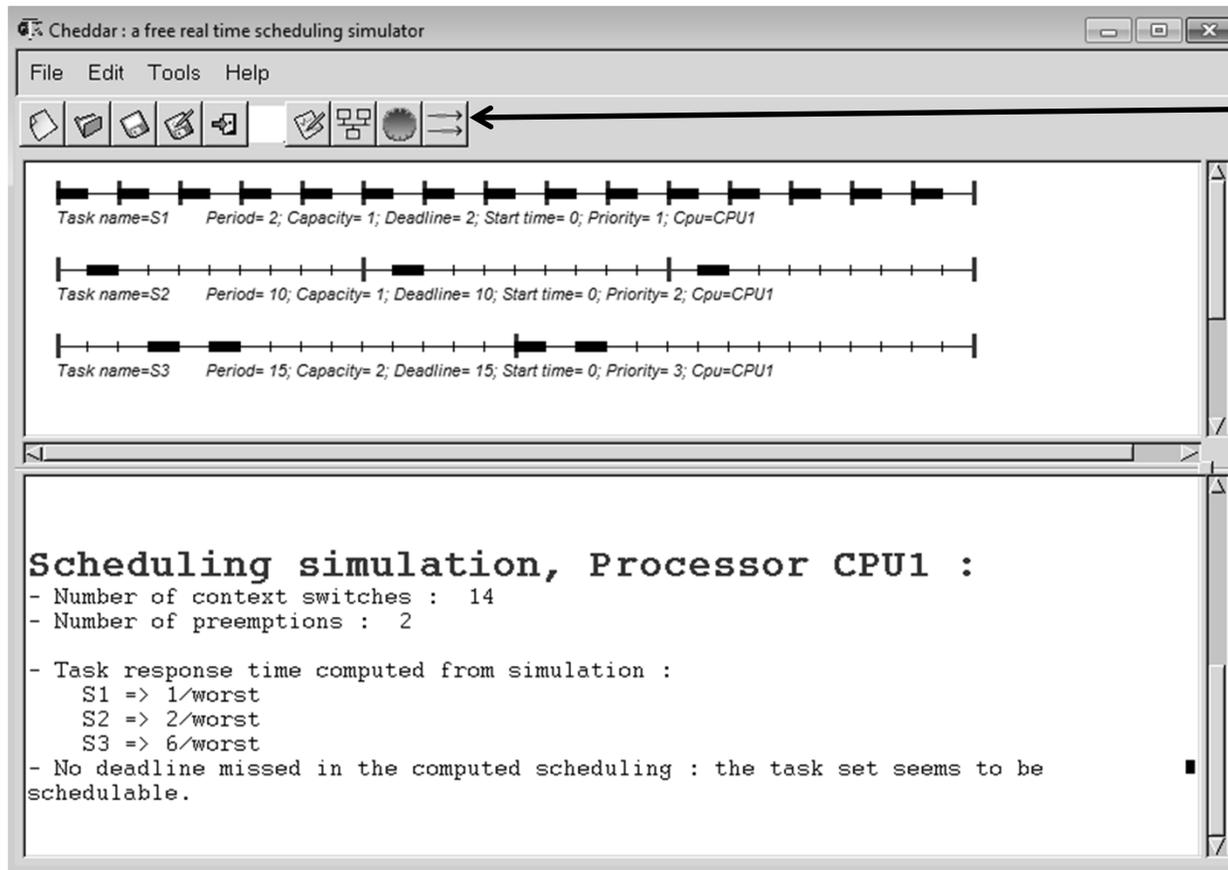
# Using Cheddar [Basics]

- Download for Windows [\[here\]](#)
- Use “Edit” to Start
- Start with Update Processors
- Add it
- Update Address Spaces, Add it
- Update Tasks, Add  $S_1 \dots S_n$
- Note Cheddar Runs over LCM



# Simulation

- Hit Simulation button to Start
- Calculates LCM, Runs, Produces Timing Diagram and Summary



Simulation Button

Timing Diagram

Summary – Note the conclusion “seems”

# Feasibility Test

- Hit Feasibility button to Test
- For RM Policy, Cheddar Uses the RM LUB
- For All Policies, Cheddar Provides Worst-Case Analysis

## Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

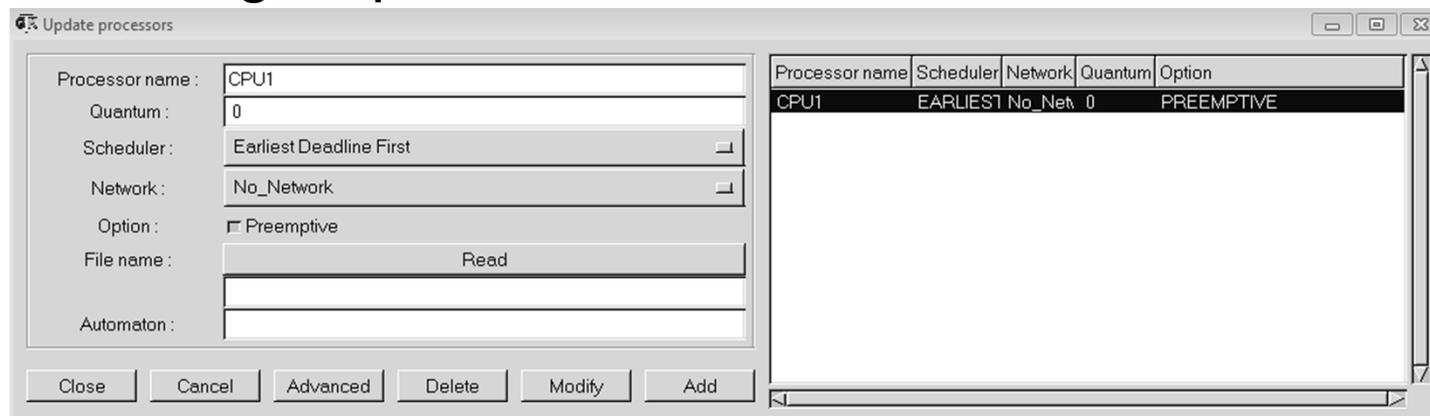
- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with RM, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 0.77976 (see [1], page 16, theorem 8).

RM Policy Example

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
  - S3 => 6
  - S2 => 2
  - S1 => 1
- All task deadlines will be met : the task set is schedulable.

## ■ Change Update Processors to EDF



# Run Again with EDF to Compare

- Priorities are Dynamic, So Just Change Processor Scheduler Policy, Re-Run Simulation and Feasibility

## Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
  - S1 => 1
  - S2 => 8
  - S3 => 13
- All task deadlines will be met : the task set is schedulable.

Note EDF

## Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 1.00000 (see [7]).

2) Feasibility test based on worst case task response time :

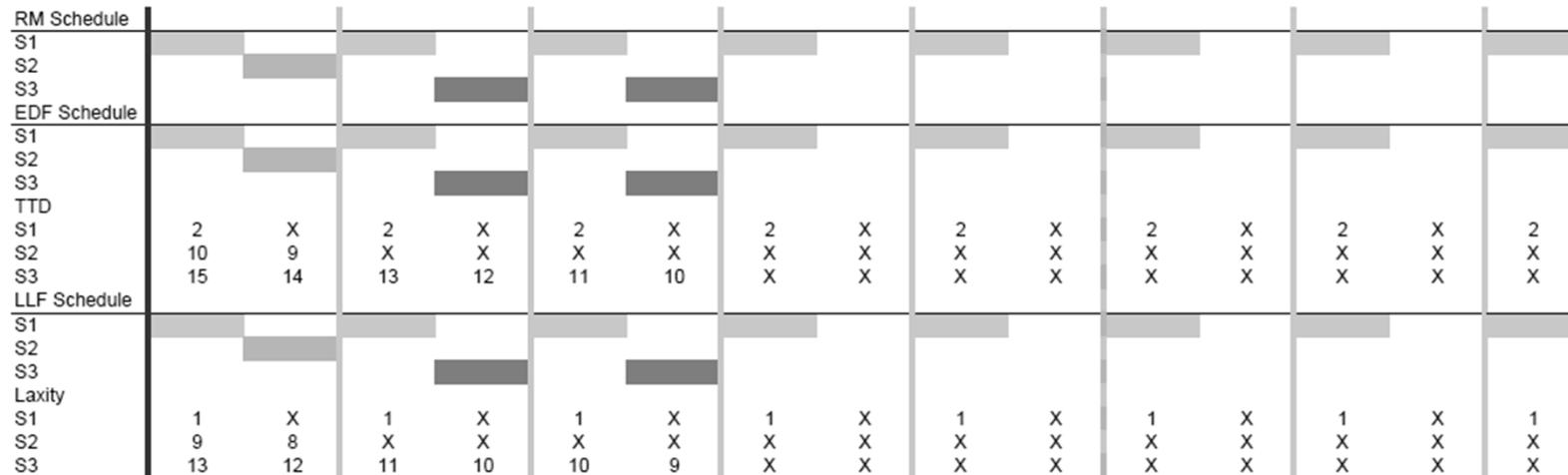
- Bound on task response time :
  - S1 => 1
  - S2 => 8
  - S3 => 13
- All task deadlines will be met : the task set is schedulable.

Note LLF

# Example-0 Timing Diagram

## ■ RM, EDF, LLF Succeed, 73.33% CPU Utilization

Example 0    T1    2    C1    1    U1    0.5    LCM =    30  
                  T2    10    C2    1    U2    0.1  
                  T3    15    C3    2    U3    0.133333    Utot =    0.733333

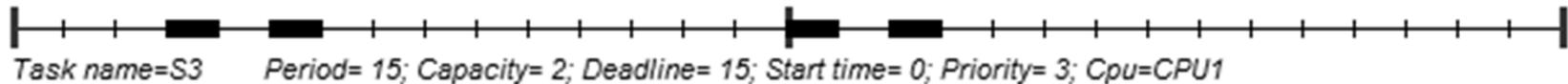
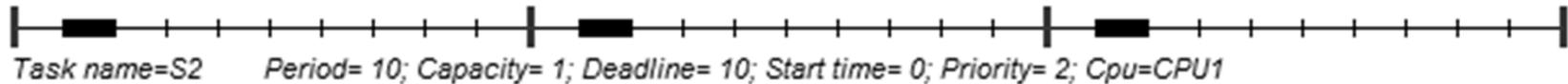
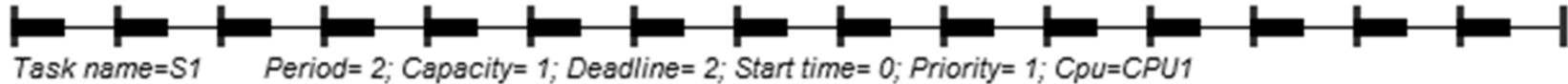


### Scheduling simulation, Processor CPU1 :

- Number of context switches : 14
- Number of preemptions : 2
- Task response time computed from simulation :
  - S1 => 1/worst
  - S2 => 2/worst
  - S3 => 6/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

# Example-0 Cheddar RTSS

## ■ Download Cheddar RT Analyzer, Example-0 XML



### Scheduling feasibility, Processor CPU1 :

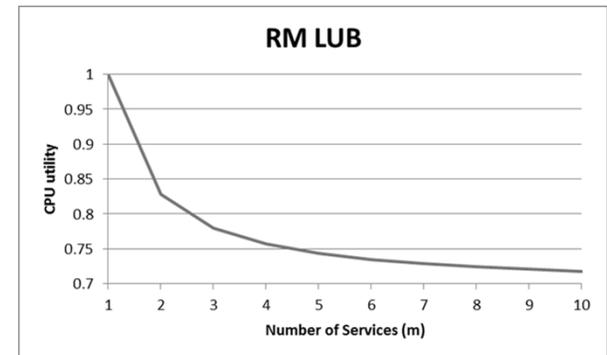
1) Feasibility test based on the processor utilization factor :

$$U = \sum_{i=1}^m (C_i / T_i) \leq m(2^{\frac{1}{m}} - 1)$$

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with RM, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 0.77976 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
  - S3 => 6
  - S2 => 2
  - S1 => 1
- All task deadlines will be met : the task set is schedulable.



# Example-1 Timing Diagram

## ■ RM FAILS, EDF, LLF Succeed, 98.57% CPU Utilization

<b>Example 1</b>	T1	2	C1	1	U1	0.5	LCM =	70		
	T2	5	C2	1	U2	0.2				
	T3	7	C3	2	U3	0.285714	Utot =	0.985714		
<b>RM Schedule</b>										
S1	[shaded]		[shaded]		[shaded]		????????			
S2	[shaded]		[shaded]		[shaded]		????????			
S3	[shaded]		[shaded]		[shaded]			LATE		
<b>EDF Schedule</b>										
S1	[shaded]		[shaded]		[shaded]		[shaded]		[shaded]	
S2	[shaded]		[shaded]		[shaded]		[shaded]		[shaded]	
S3	[shaded]		[shaded]		[shaded]		[shaded]		[shaded]	
<b>TTD</b>										
S1	2	X	2	X	2	X	2	X	2	X
S2	5	4	X	X	X	5	4	3	X	X
S3	7	6	5	4	3	2	X	7	6	5
<b>LLF Schedule</b>										
S1	[shaded]		[shaded]		[shaded]		[shaded]		[shaded]	
S2	[shaded]		[shaded]		[shaded]		[shaded]		[shaded]	
S3	[shaded]		[shaded]		[shaded]		[shaded]		[shaded]	
<b>Laxity</b>										
S1	1	X	1	X	1	X	1	X	1	X
S2	4	3	X	X	X	4	3	2	X	X
S3	5	4	3	2	2	1	X	5	4	3

### Scheduling simulation, Processor CPU1 :

- Number of context switches : 68
- Number of preemptions : 10
- Task response time computed from simulation :
  - S1 => 1/worst
  - S2 => 2/worst
  - S3 => 8/worst , missed its deadline (deadline = 7 ; completion time = 8)
- Some task deadlines will be missed : the task set is not schedulable.

# Example-1 Cheddar RTSS

## ■ RM Not Feasible by LUB or by Inspection over LCM

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 70 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.98571 (see [1], page 6).
- Processor utilization factor with period is 0.98571 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable is more than 0.77976 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
  - S3 => 8, missed its deadline (deadline = 7)
  - S2 => 2
  - S1 => 1
- Some task deadlines will be missed : the task set is not schedulable.

## ■ EDF?

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

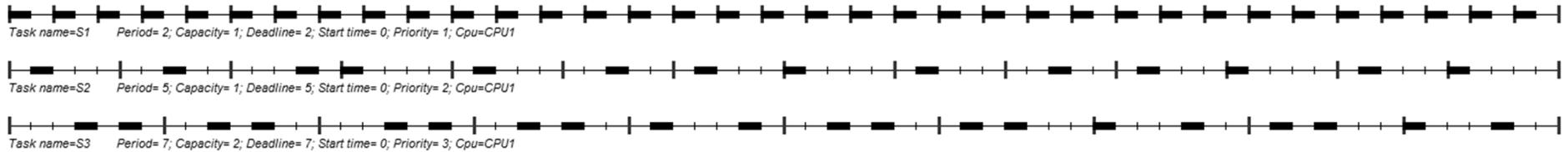
- The base period is 70 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.98571 (see [1], page 6).
- Processor utilization factor with period is 0.98571 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.98571 is equal or less 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

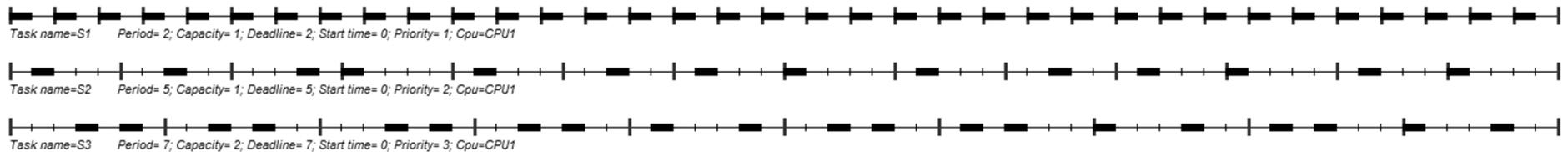
- Bound on task response time :
  - S1 => 1
  - S2 => 4
  - S3 => 6
- All task deadlines will be met : the task set is schedulable.

# Example-1 Cheddar RTSS

## ■ EDF Simulation over LCM of 70



## ■ LLF Simulation over LCM of 70



## ■ Worst Case Feasibility Test

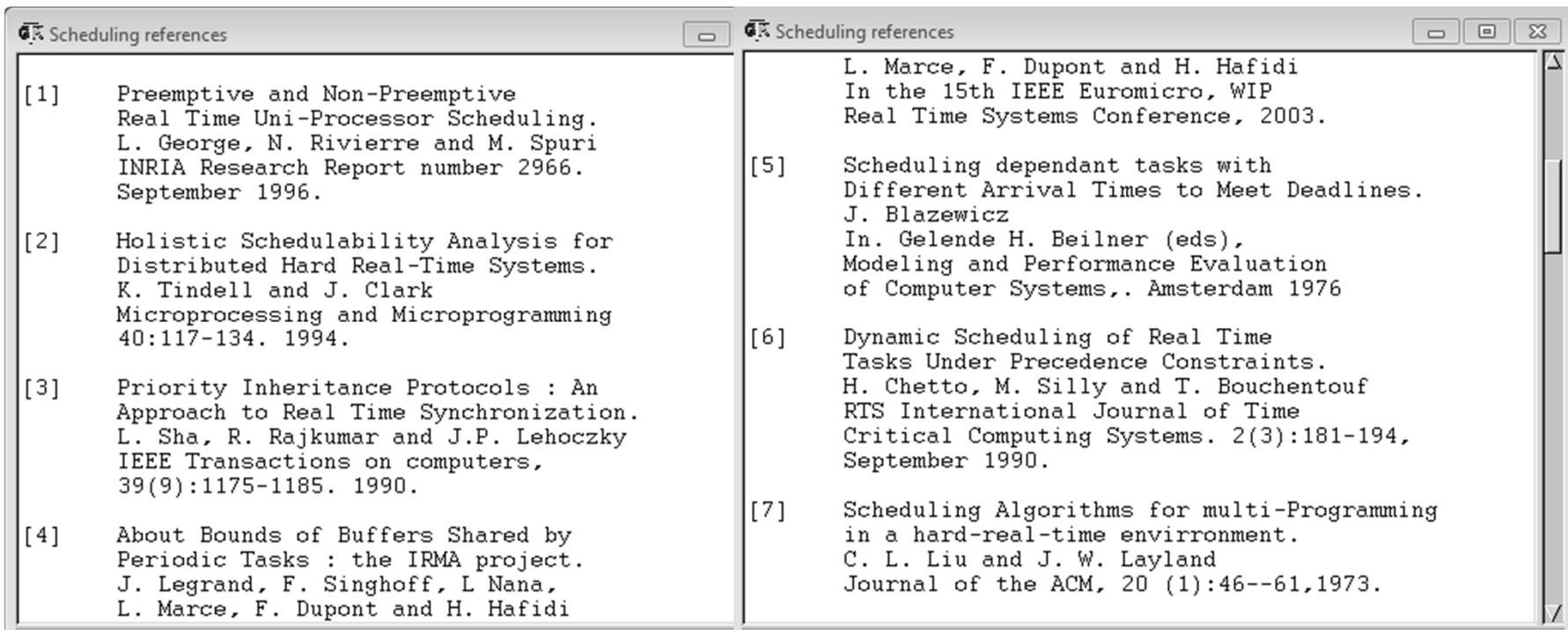
- Fixed Priority (RM Policy) FAILS LUB and WC Feasibility Test (Scheduling Point or Completion Test)
- Dynamic Priority Succeeds by Two Methods

# Review Remaining Examples

- [http://mercury.pr.erau.edu/~siewerts/cec450/documents/](http://mercury.pr.erau.edu/~siewerts/cec450/documents/Timing_Diagrams/)  
[Timing\\_Diagrams/](http://mercury.pr.erau.edu/~siewerts/cec450/documents/Timing_Diagrams/)
- As Noted in Liu and Layland, Static Priority Policy May Not be Feasible in Cases where Dynamic Priority Policy is Feasible
- Are Feasibility and Safety Synonymous?
- Is it Wise to have Zero Margin?
- Have We Accounted for Context Switch Overhead and ISR Latency?

# Cheddar References

- Help, Scheduling References
- References Used to Build Cheddar – [Here](#)
- General References - [Here](#)



The image shows a screenshot of a window titled "Scheduling references" with a scrollable list of seven references. The references are numbered [1] through [7].

[1] Preemptive and Non-Preemptive Real Time Uni-Processor Scheduling. L. George, N. Rivierre and M. Spuri INRIA Research Report number 2966. September 1996.

[2] Holistic Schedulability Analysis for Distributed Hard Real-Time Systems. K. Tindell and J. Clark Microprocessing and Microprogramming 40:117-134. 1994.

[3] Priority Inheritance Protocols : An Approach to Real Time Synchronization. L. Sha, R. Rajkumar and J.P. Lehoczky IEEE Transactions on computers, 39(9):1175-1185. 1990.

[4] About Bounds of Buffers Shared by Periodic Tasks : the IRMA project. J. Legrand, F. Singhoff, L Nana, L. Marce, F. Dupont and H. Hafidi L. Marce, F. Dupont and H. Hafidi In the 15th IEEE Euromicro, WIP Real Time Systems Conference, 2003.

[5] Scheduling dependant tasks with Different Arrival Times to Meet Deadlines. J. Blazewicz In. Gelende H. Beilner (eds), Modeling and Performance Evaluation of Computer Systems,. Amsterdam 1976

[6] Dynamic Scheduling of Real Time Tasks Under Precedence Constraints. H. Chetto, M. Silly and T. Bouchentouf RTS International Journal of Time Critical Computing Systems. 2(3):181-194, September 1990.

[7] Scheduling Algorithms for multi-Programming in a hard-real-time environment. C. L. Liu and J. W. Layland Journal of the ACM, 20 (1):46--61,1973.